REMARKS

This is intended as a full and complete response to the Office Action dated July 2, 2003, having a shortened statutory period for response set to expire on October 2, 2003. Please reconsider the claims pending in the application for reasons discussed below.

Claims 1 - 28 are pending in the application and are shown above. Claims 1-6, 12-17, 19-24 and 29-39 remain pending following entry of this response. Claims 7-9, 18, 25 and 26 have been cancelled by Applicants without prejudice and re-presented in independent form as claim 29-31, and 34-36, respectively. Claims 10, 11, 27, and 28 have been cancelled and re-presented as claims 32, 33, 37, and 38. Applicants submit that the new claims do not introduce new matter and are commensurate in scope with their cancelled counterparts. Accordingly, Applicants submit that the new claims are entitled to a full range of equivalents for each of the recited elements. Reconsideration of the rejected claims is requested for reasons presented below.

The abstract of the disclosure is objected to because it does not enable one to quickly determine from a cursory inspection the nature and gist of the technical disclosure as required by 37 CFR 1.72(b). Applicants believe the abstract, as filed, is appropriate and does not require amendment. MPEP 608.01(b) states that the abstract may not exceed 150 words and that it is not intended nor designed for use in interpreting the scope or meaning of the claims, 37 CFR 1.72(b). Applicants submit that the abstract satisfies these requirements. While Applicants acknowledge that the present application discloses patentable subject matter which may be different from, or in addition to, what is stated in the abstract, Applicants are not aware of a requirement which necessitates amending the abstract. If the Examiner still disagrees and insists upon an amendment, Applicants will submit to an amendment with the understanding that such an amendment is in no way limiting of the claims, either currently or subsequently pending.

Claims 1-6, 12-17, and 19-24 stand rejected under 35 USC § 102(b) as being anticipated by *Bryg et al.* (US Pat 5,586,297, hereinafter *Bryg*). Applicants respectfully traverse the rejection.

Bryg discloses a method of managing performance by I/O adapters of coherent direct memory access (DMA) write transactions for a block of data which is smaller than a cache line. The Examiner suggests that the claimed element of sending a cache line to at least one of a plurality of processors in the shared memory multiple processor computer system to update the at least one of a plurality of processors is taught by *Bryg* at column 4, lines 10 through 13. The Applicants respectfully point out that the cited passage explains conventional methods of performing a direct memory access write transaction, where a block of data is written from the I/O adapter to a memory location within the memory. The cache is searched to determine whether the cache contains data for the memory location and when the search determines that the cache contains data for the location, a full cache line which contains the date for the memory is purged. The cited passage describes that when DMA transactions are aligned on cache line boundaries, the entire cache line is written to the memory using several coherent sub-line writes. Each coherent sub-line write also performs a purge of the cache line in the processor caches. The passage further describes that when the processor again fetches the updated data to its cache after the first coherent sub-line write, the cache line may be purged again after later sub-line writes are complete. The passage does not in any way teach, show, or suggest sending a purged cache line from a processor to the cache of one or more other processors in a shared-memory multiple processor computer system to update the other processor(s).

Furthermore, *Bryg* is directed to simplifying coherent DMA write operations where the I/O block size is smaller than the processor cache's line size, as opposed to efficiently moving cache lines between the caches of different processors to reduce the number of cache misses and increase performance of multiple processor systems. Therefore, the claims are believed to be allowable and allowance of the same is respectfully requested.

Claims 7-11, 18, 25-28 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the

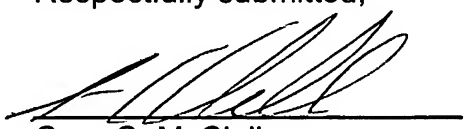
limitations of the base claim and any intervening claims. Accordingly, claims 7-9, 18, 25, 26 have been canceled and rewritten in independent form (as claims 29-31 and 34-36, respectively) and are now believed to be in condition for allowance. Further, claims 10 and 11 are dependent upon dependent claim 9, and claims 27 and 28 are dependent upon dependent claim 26. Accordingly, claims 10,11, 27, and 28 have been cancelled and rewritten in dependent form (as claims 32 and 33, dependent upon independent claim 31, and claims 37 and 38, dependent upon independent claim 36, respectively) and are now believed to be in condition for allowance.

In conclusion, the references cited by the Examiner, alone or in combination, do not teach, show, or suggest the invention as claimed.

The secondary references made of record are noted. However, it is believed that the secondary references are no more pertinent to the Applicant's disclosure than the primary references cited in the office action. Therefore, Applicant believes that a detailed discussion of the secondary references is not necessary for a full and complete response to this office action.

Having addressed all issues set out in the office action, Applicant respectfully submits that the claims are in condition for allowance and respectfully request that the claims be allowed.

Respectfully submitted,



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